

FIG. 1a

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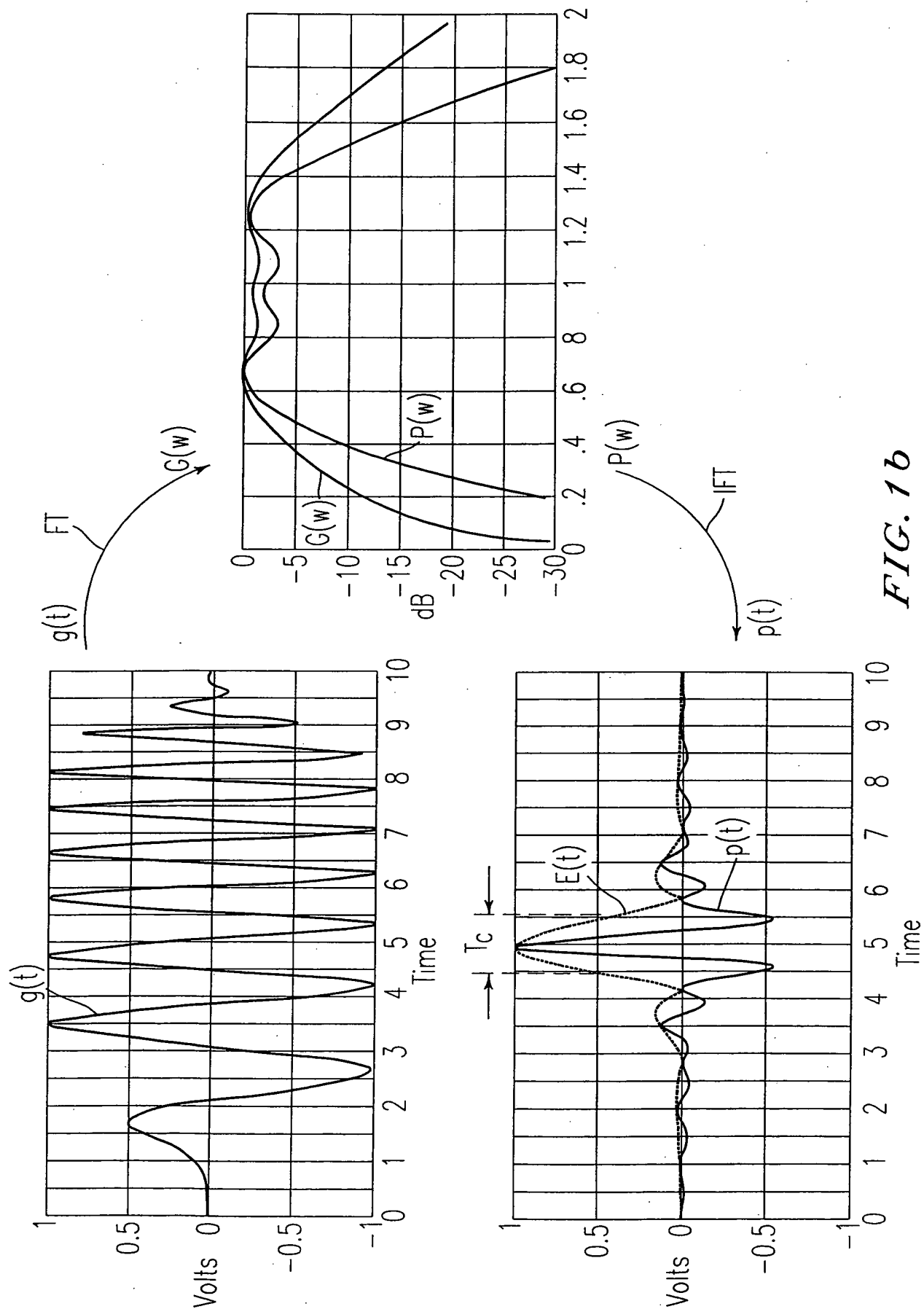


FIG. 1b

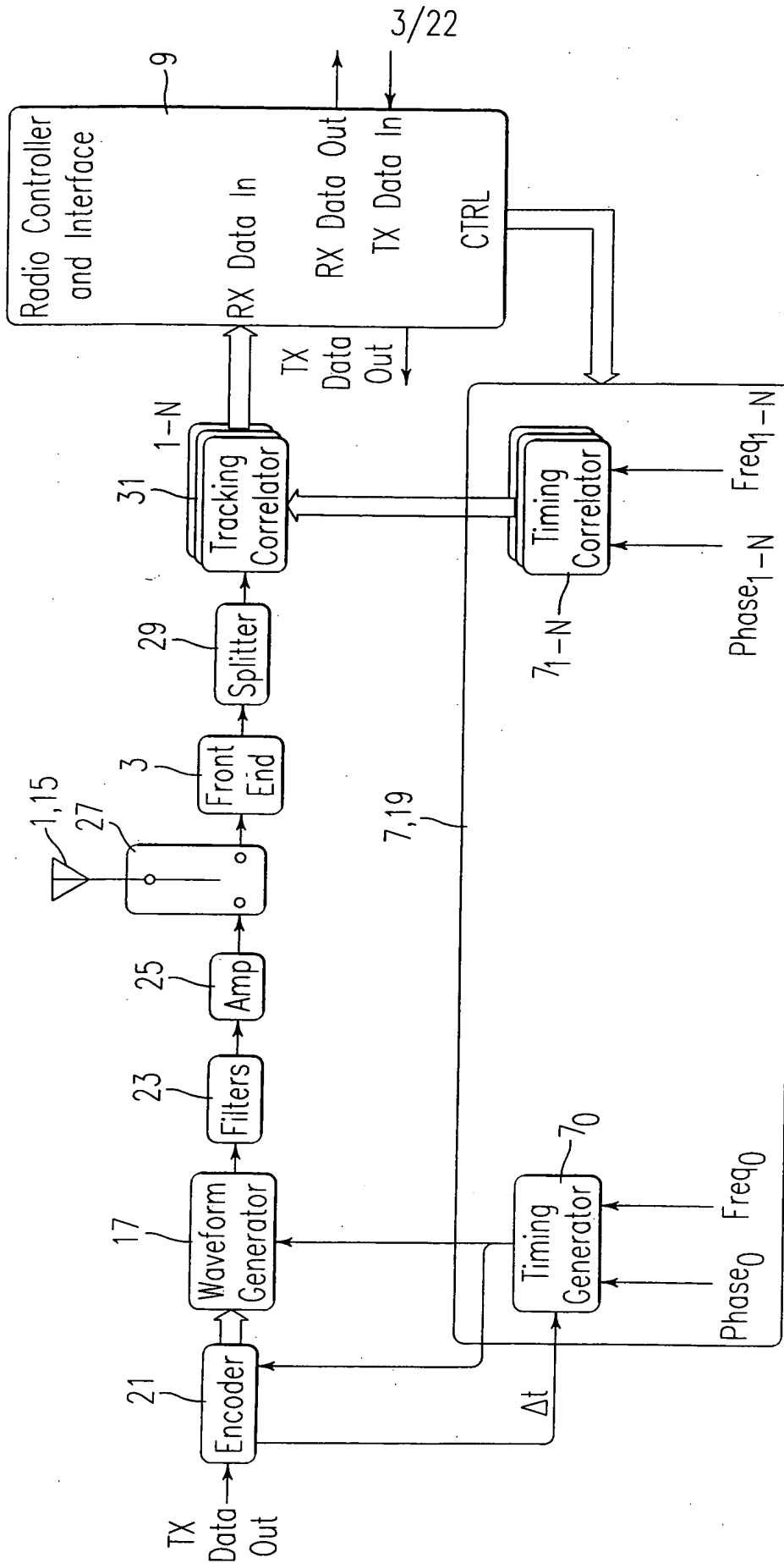


FIG. 2

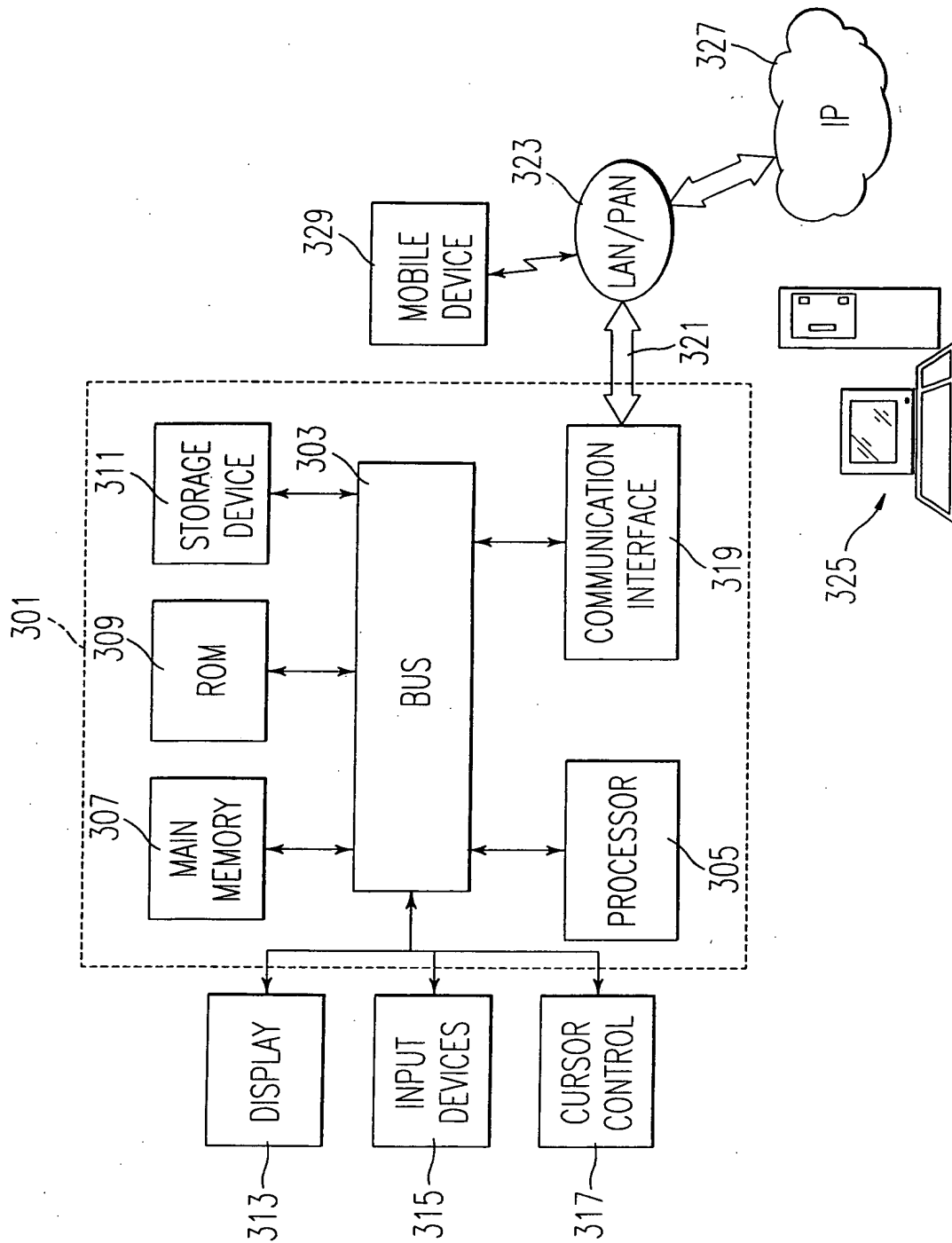


FIG. 3

FIG. 4a

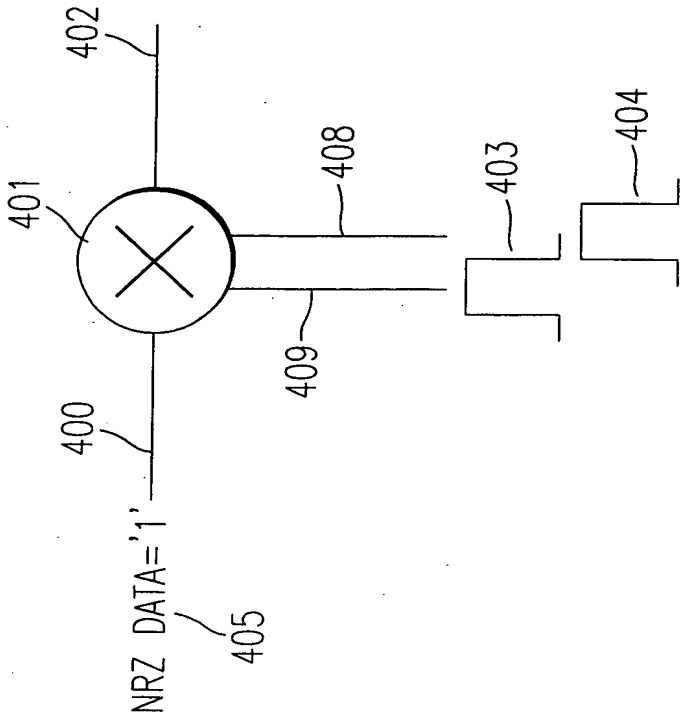
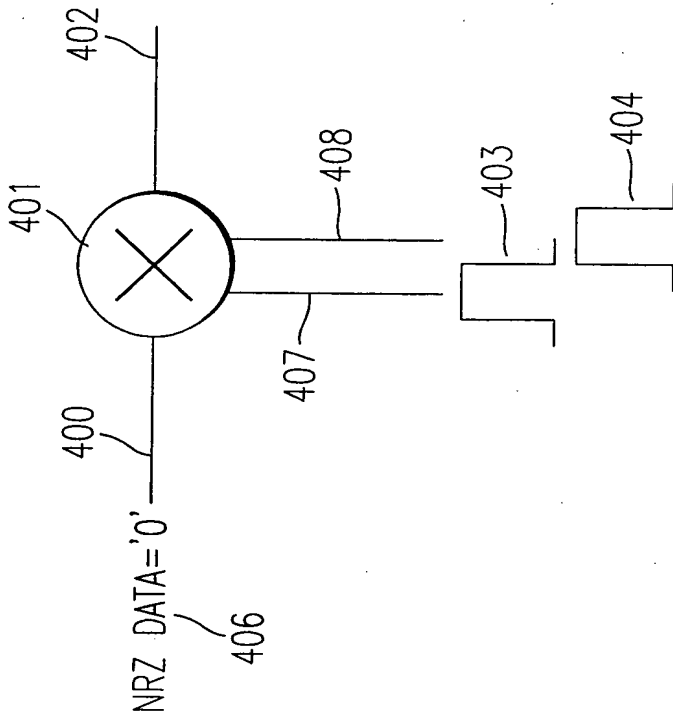
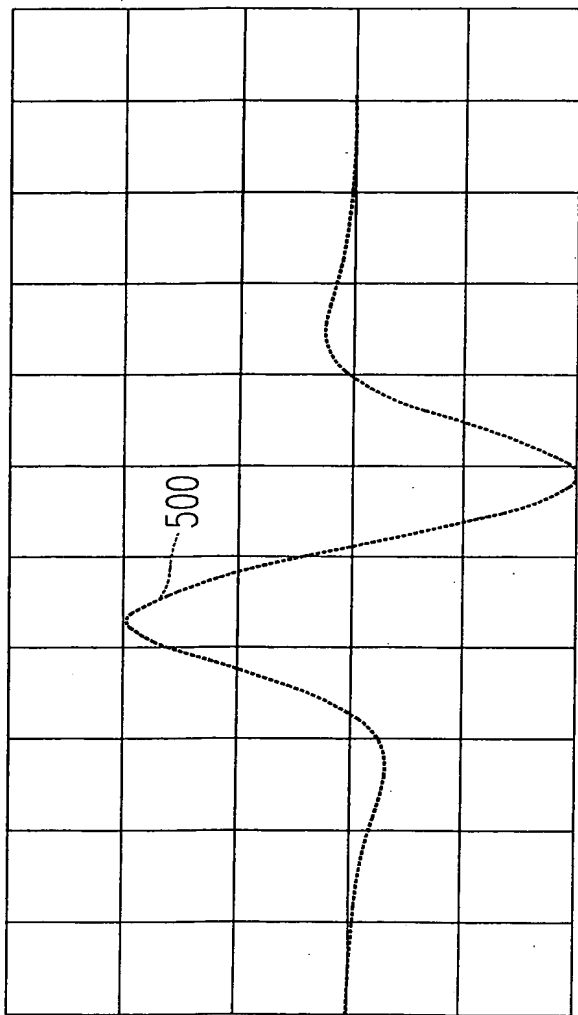


FIG. 4b

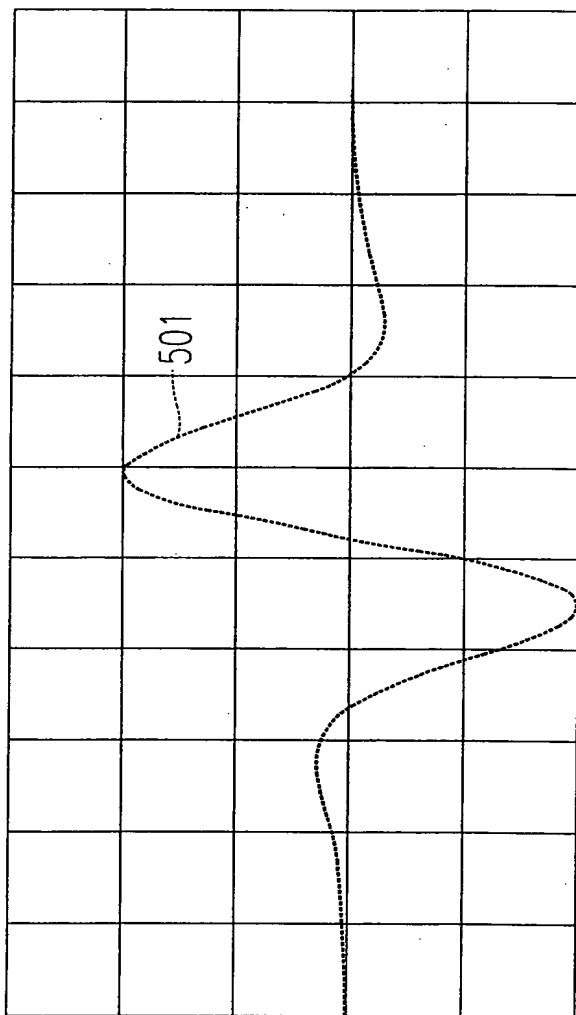


*FIG. 5a*



0

*FIG. 5b*



0

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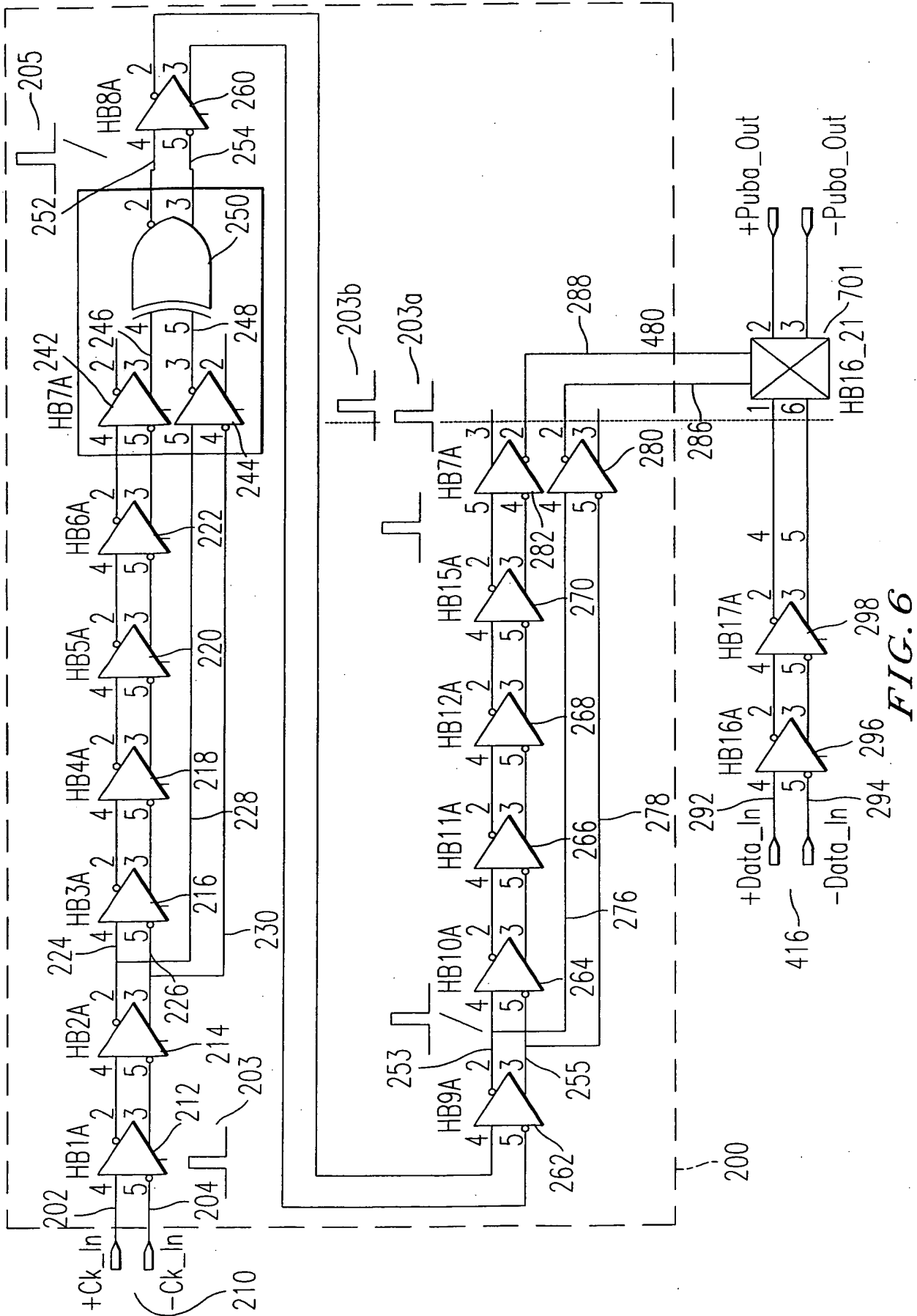


FIG. 6

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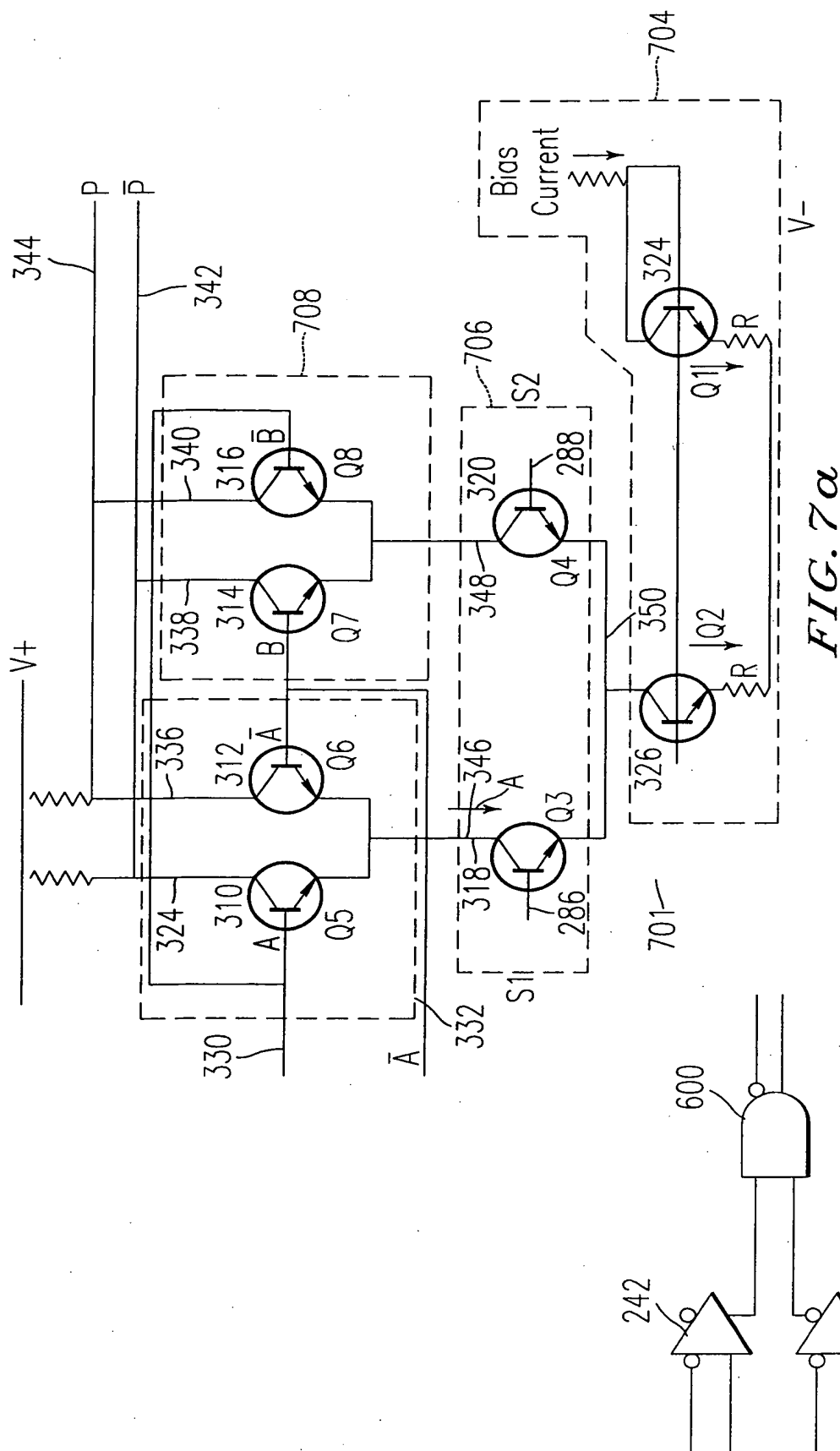


FIG. 7a

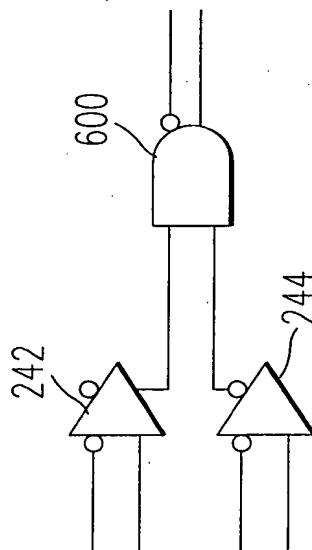
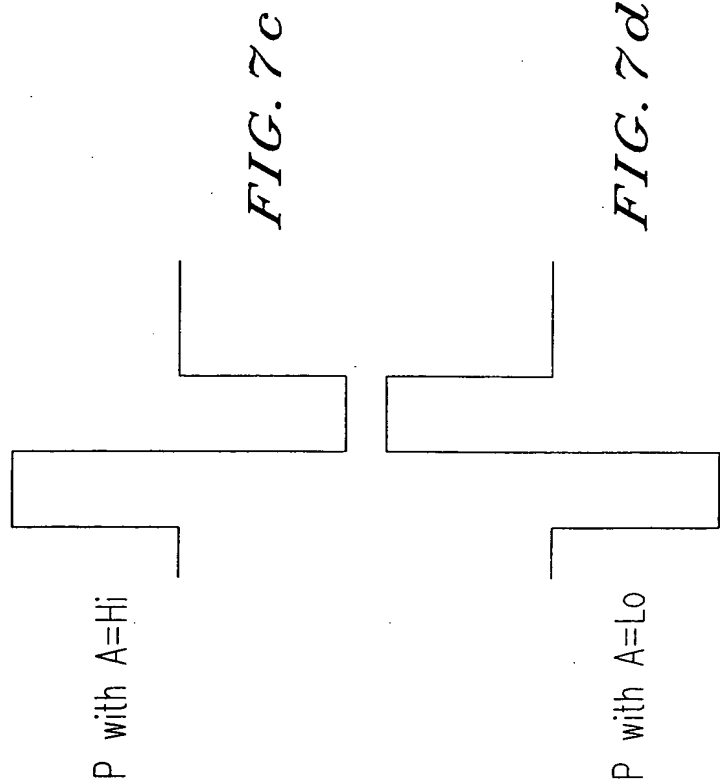
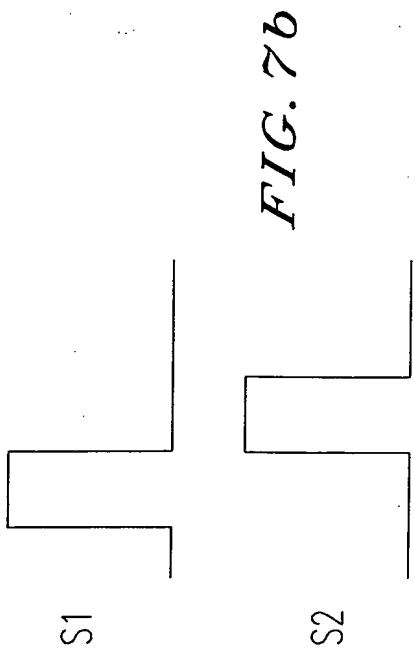
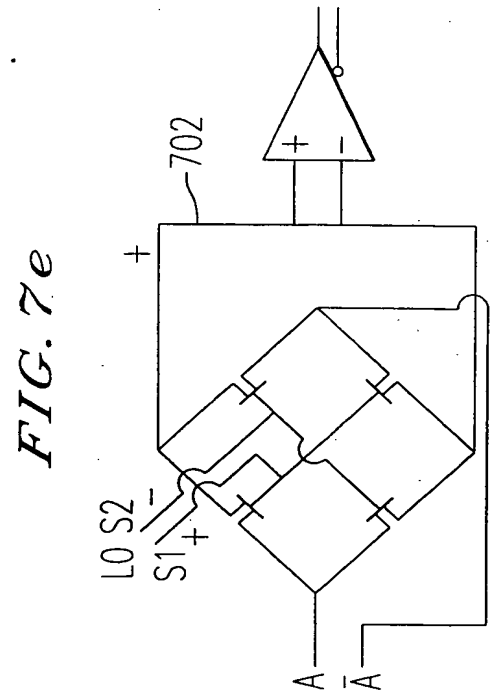
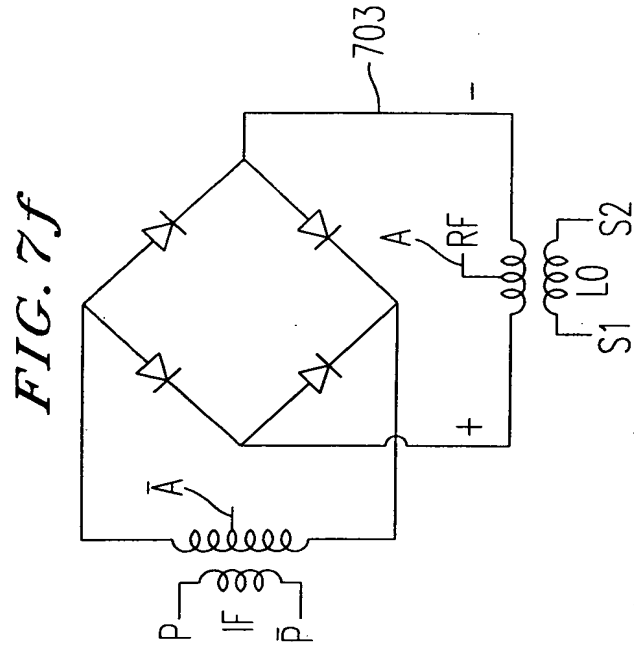


FIG. 6a



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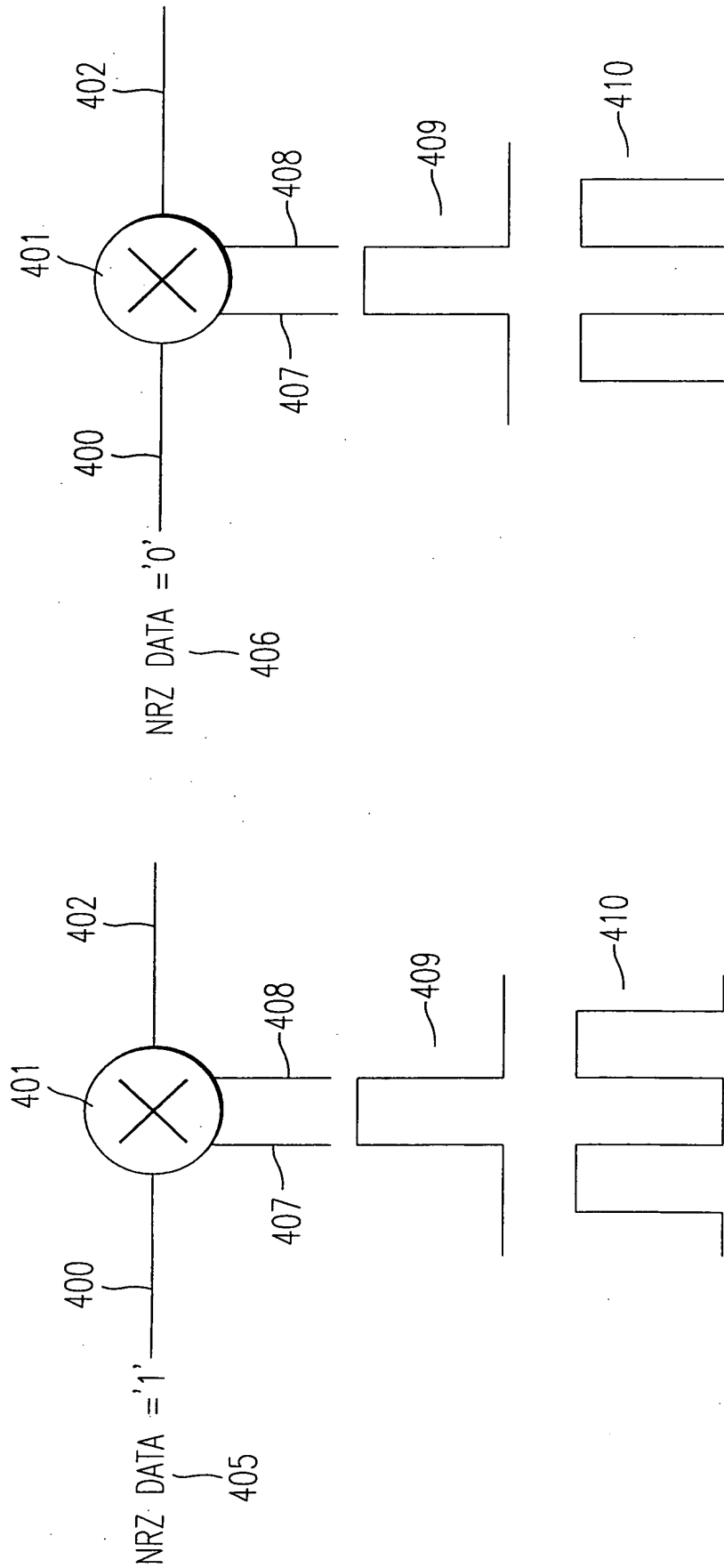
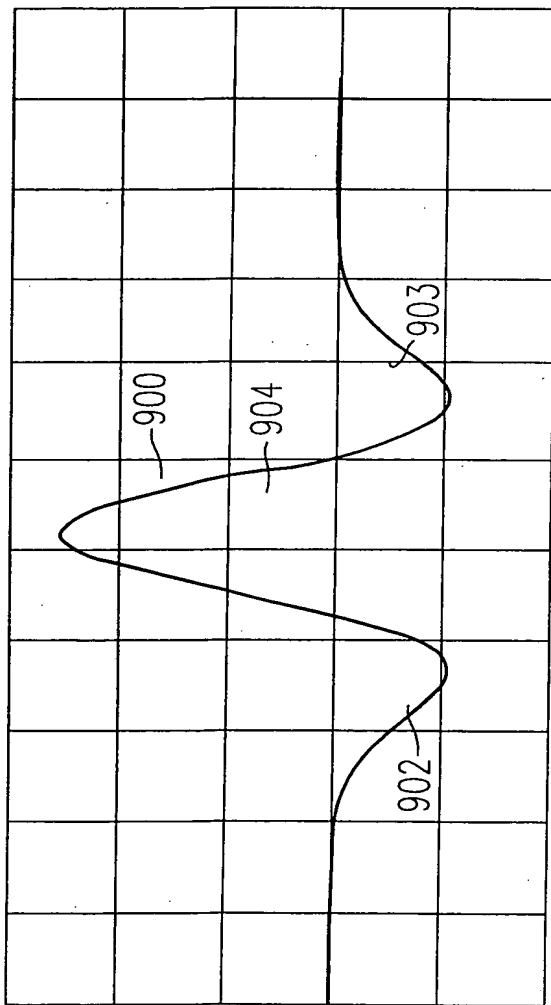


FIG. 8a

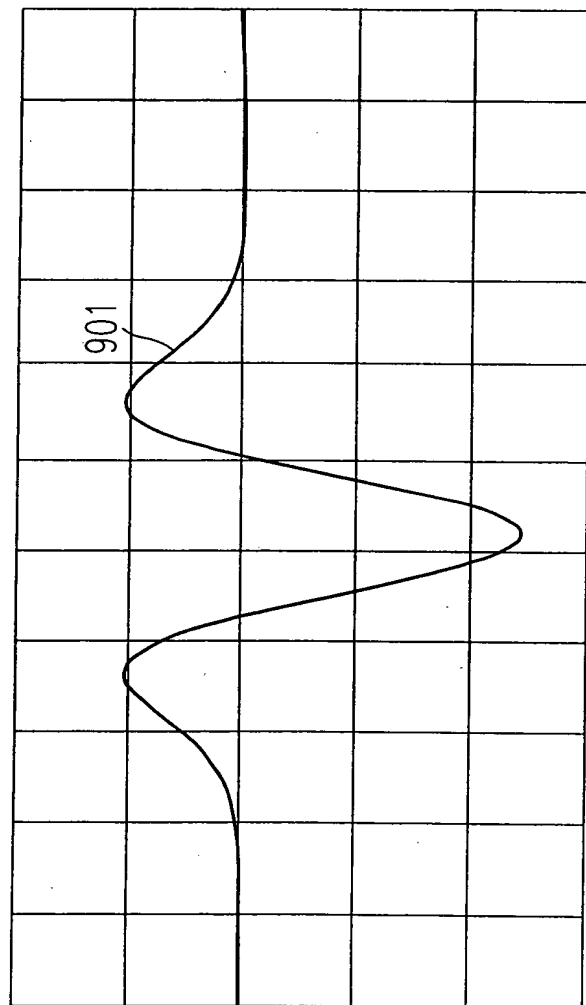
FIG. 8b

*FIG. 9a*



0

*FIG. 9b*



0

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FIG. 10a

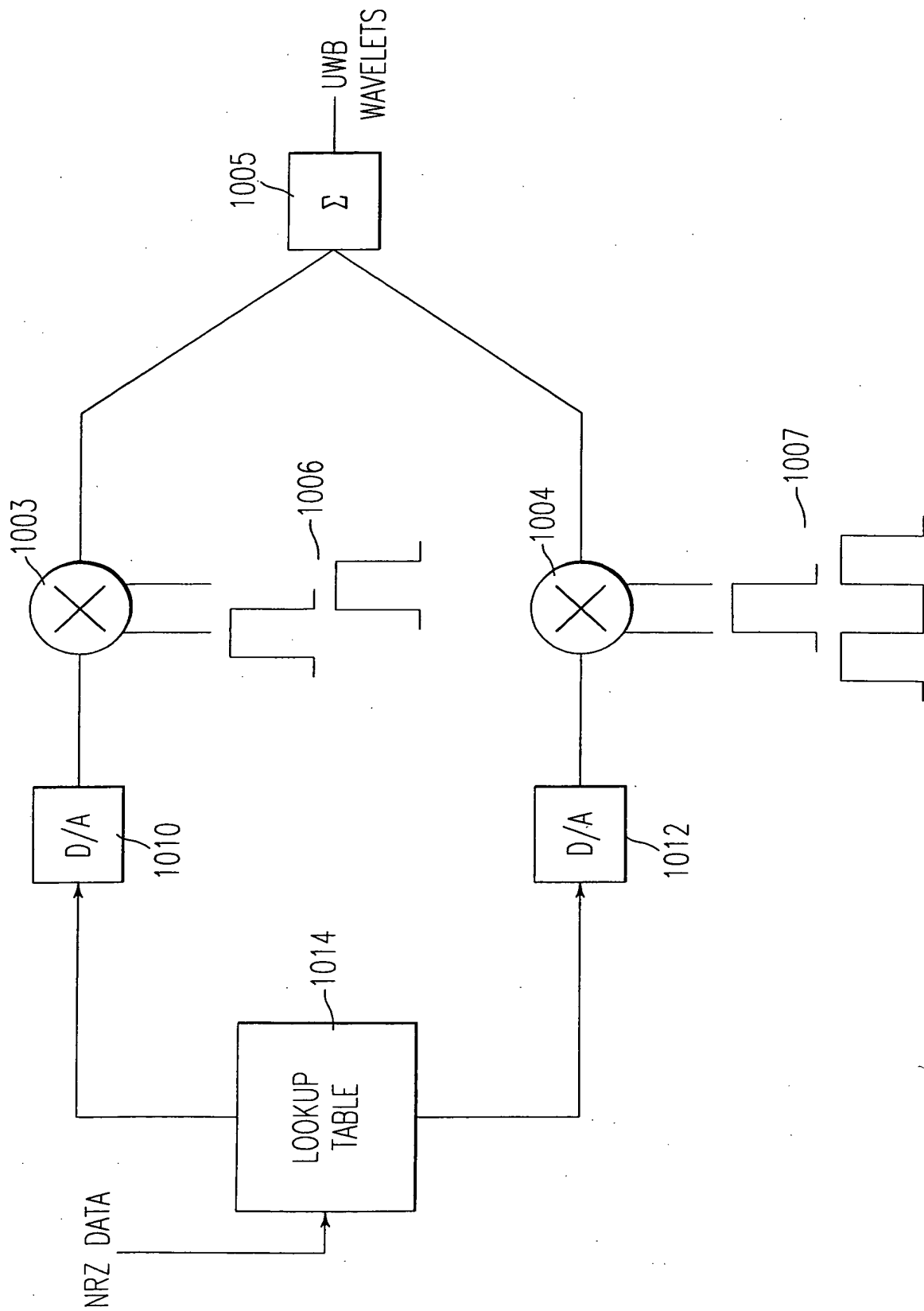
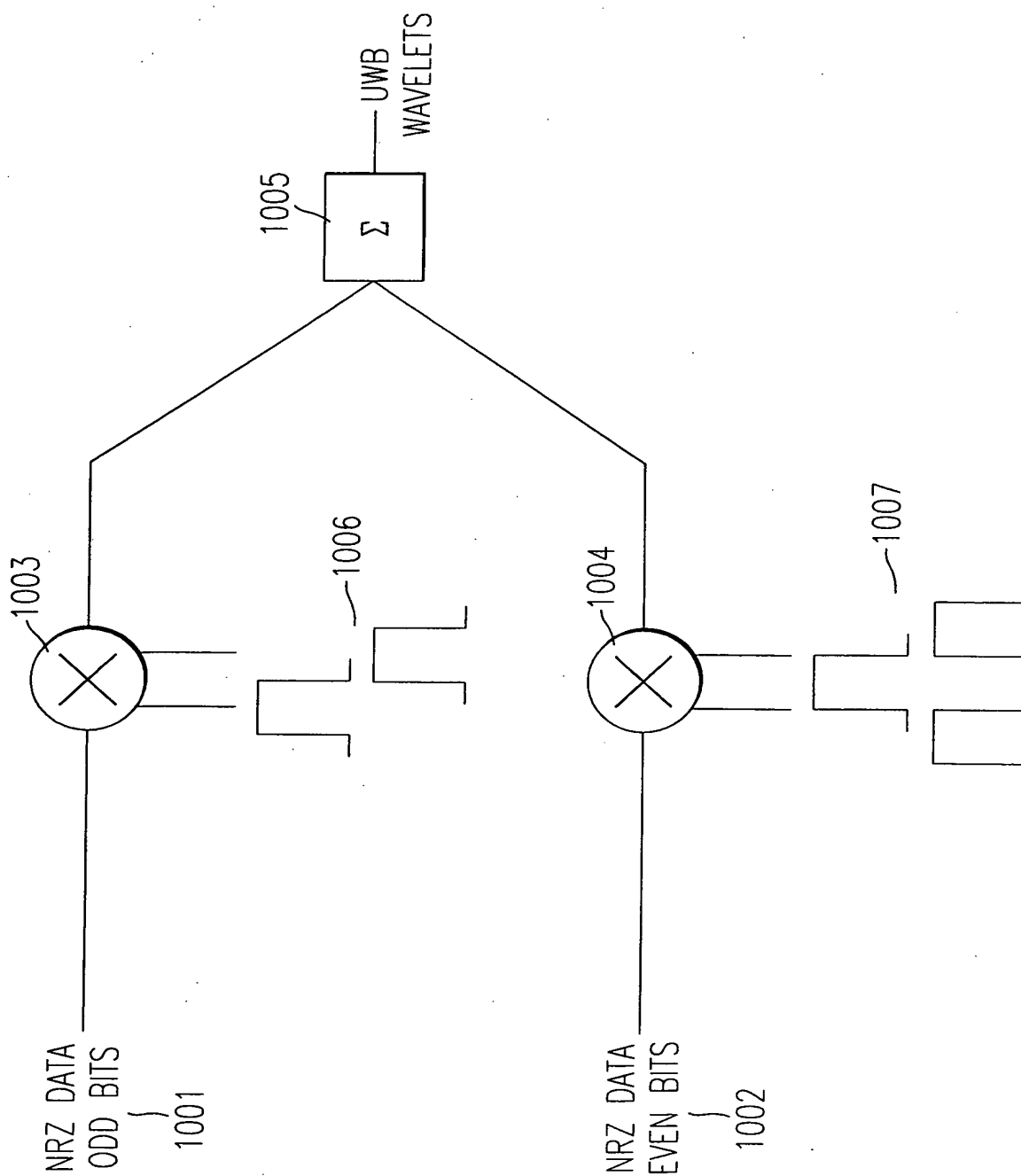
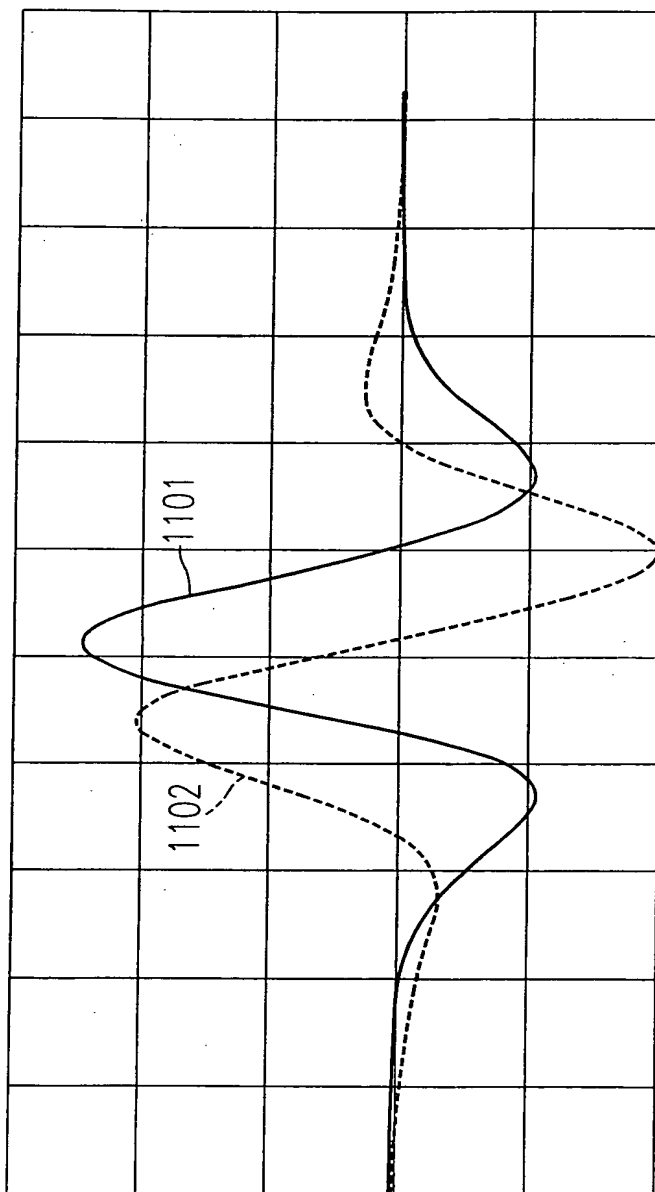


FIG. 10





*FIG. 11*

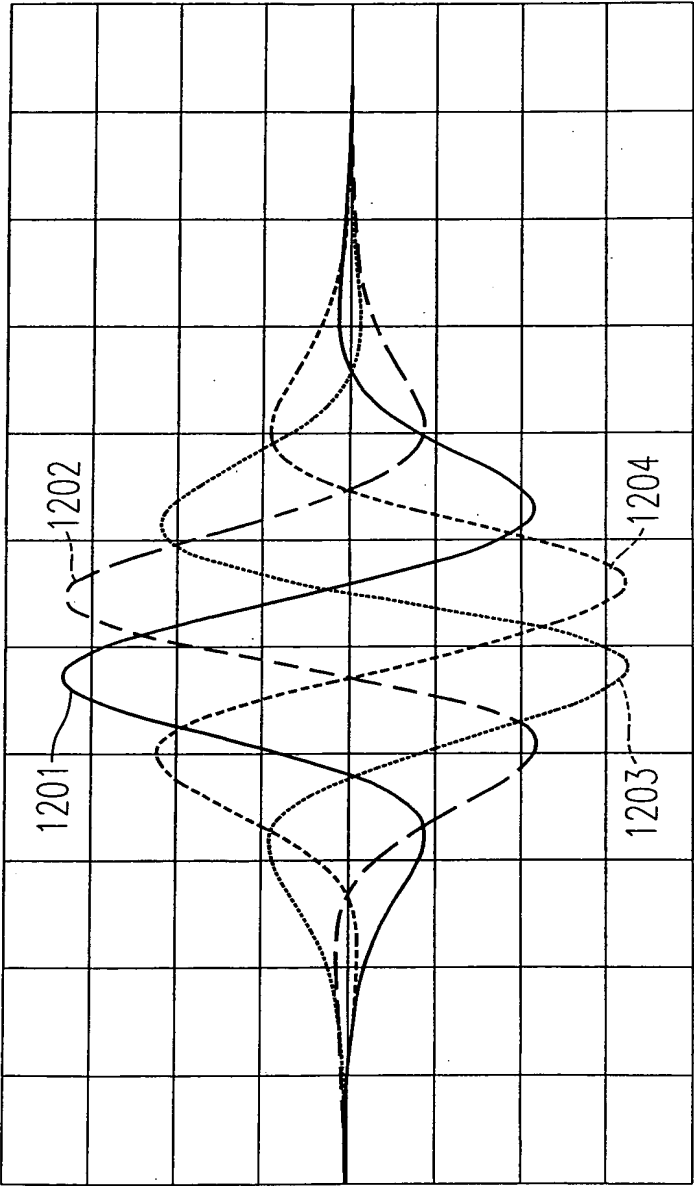


FIG. 12

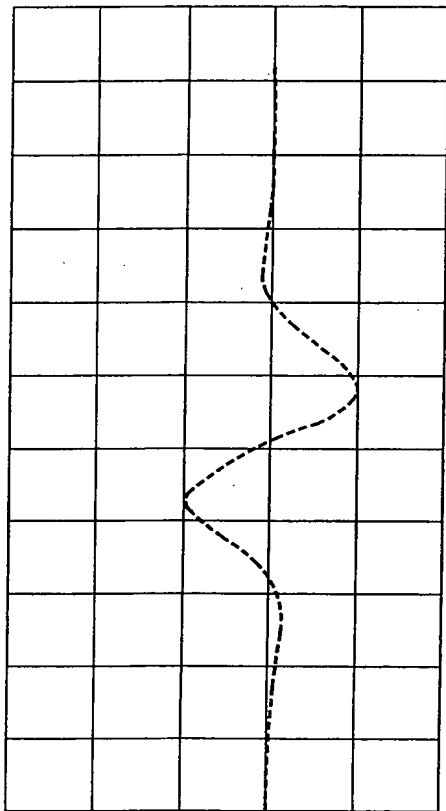


FIG. 13b

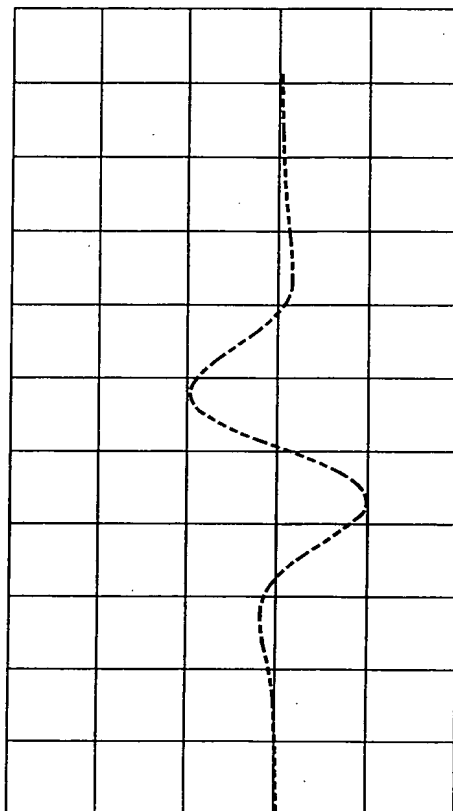


FIG. 13d

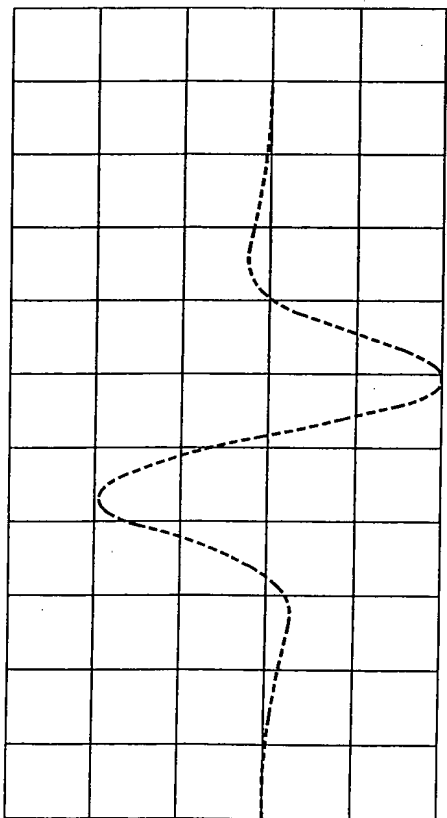


FIG. 13a

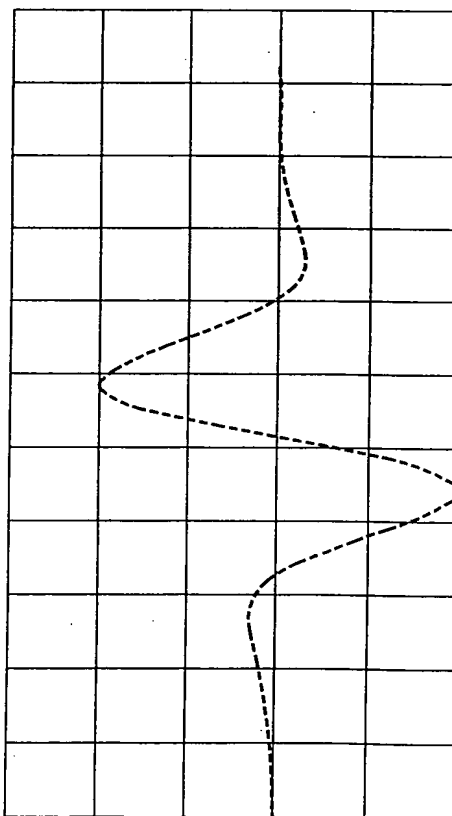
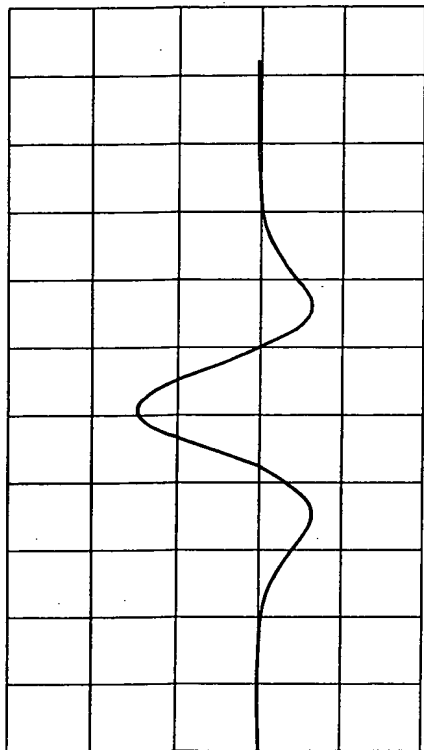


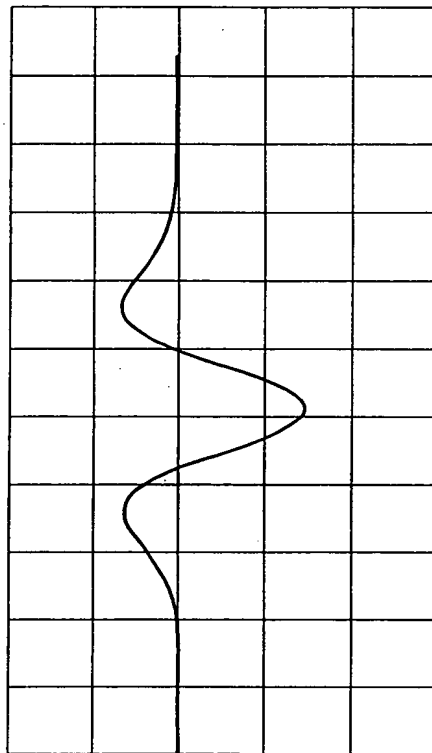
FIG. 13c



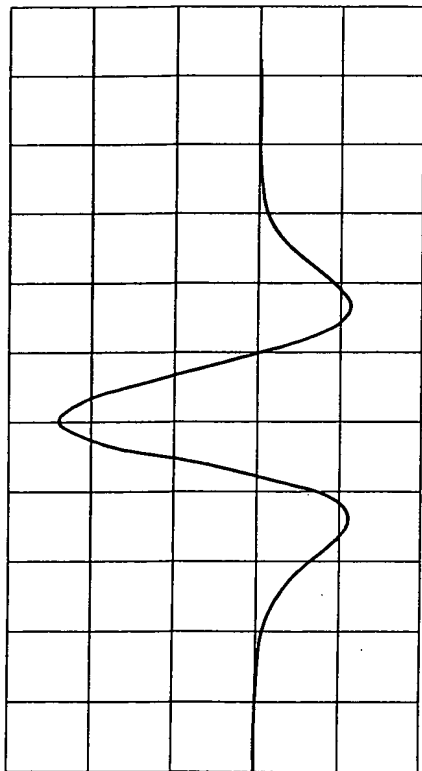
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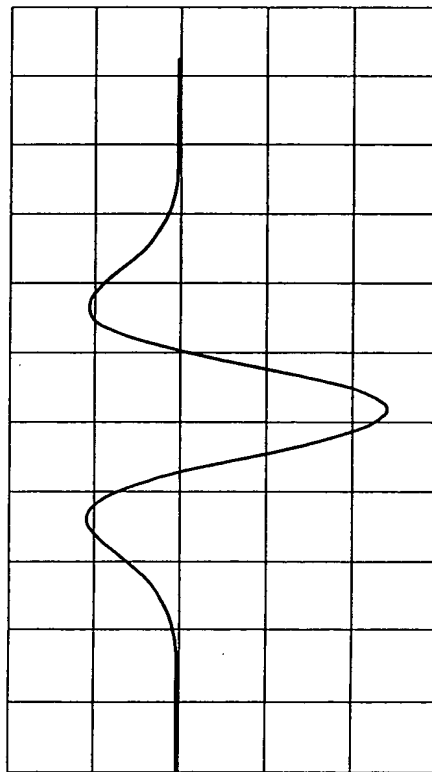
*FIG. 14b*



*FIG. 14d*



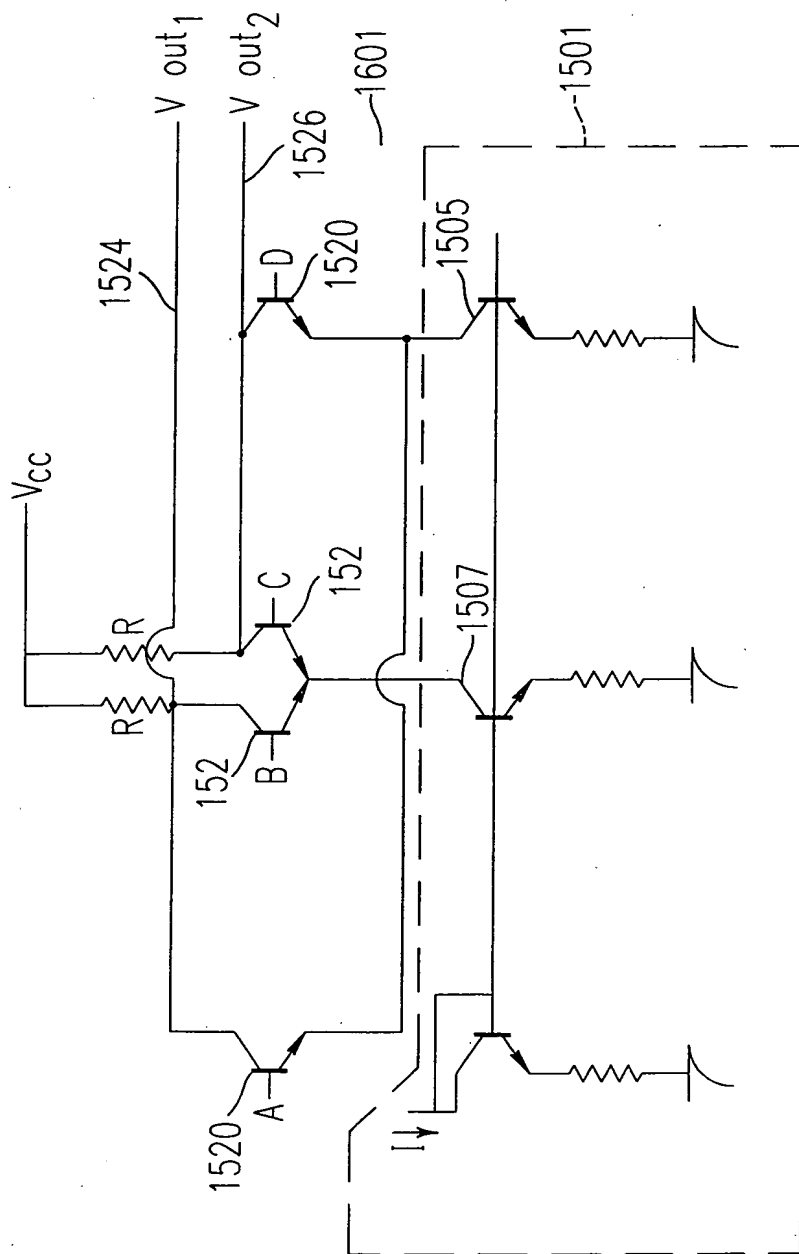
*FIG. 14a*



*FIG. 14c*

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FIG. 15



BIT	A	B	C	D	V out1	V out2
11	0	0	1	1	$2IR$	
00	1	1	0	0	$-2IR$	
10	0	0	1	0	$IR$	
01	0	1	0	0	$-IR$	

FIG. 16

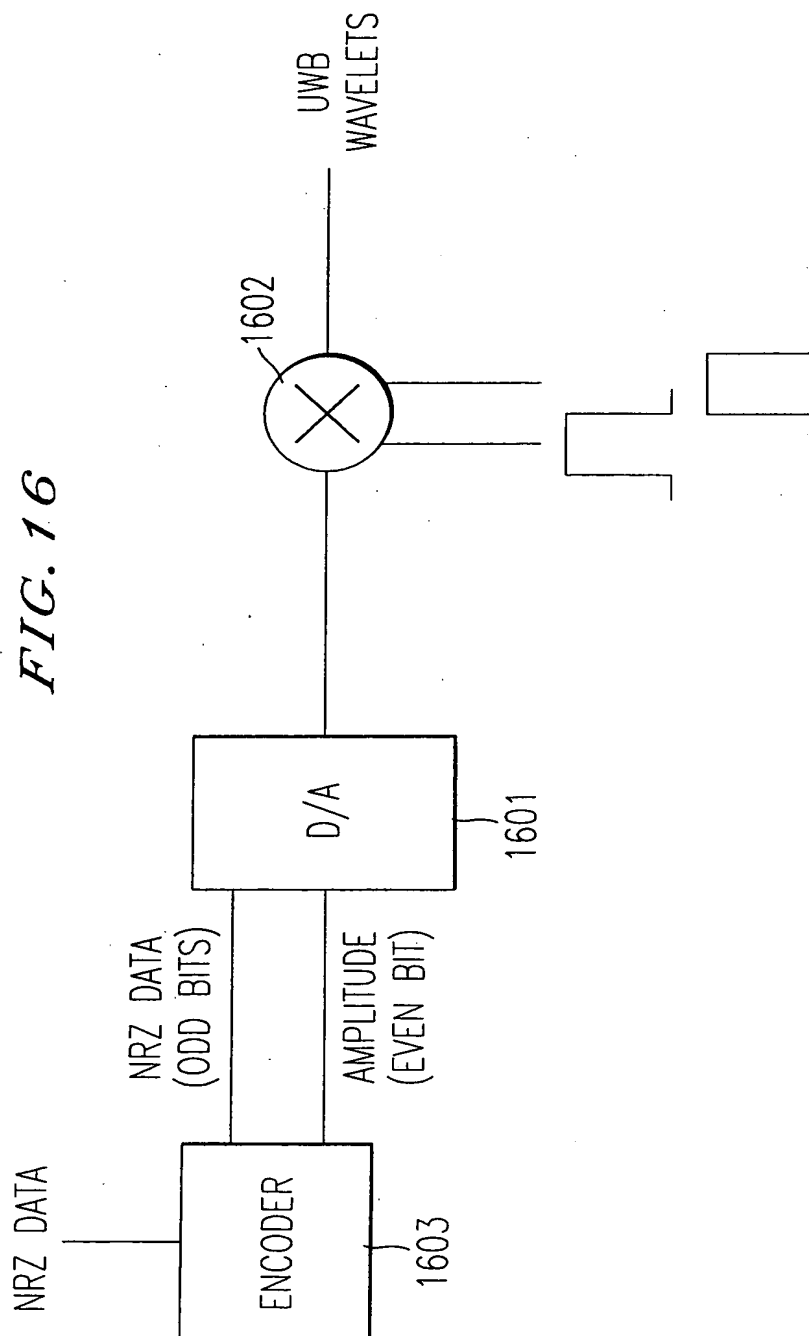


FIG. 17

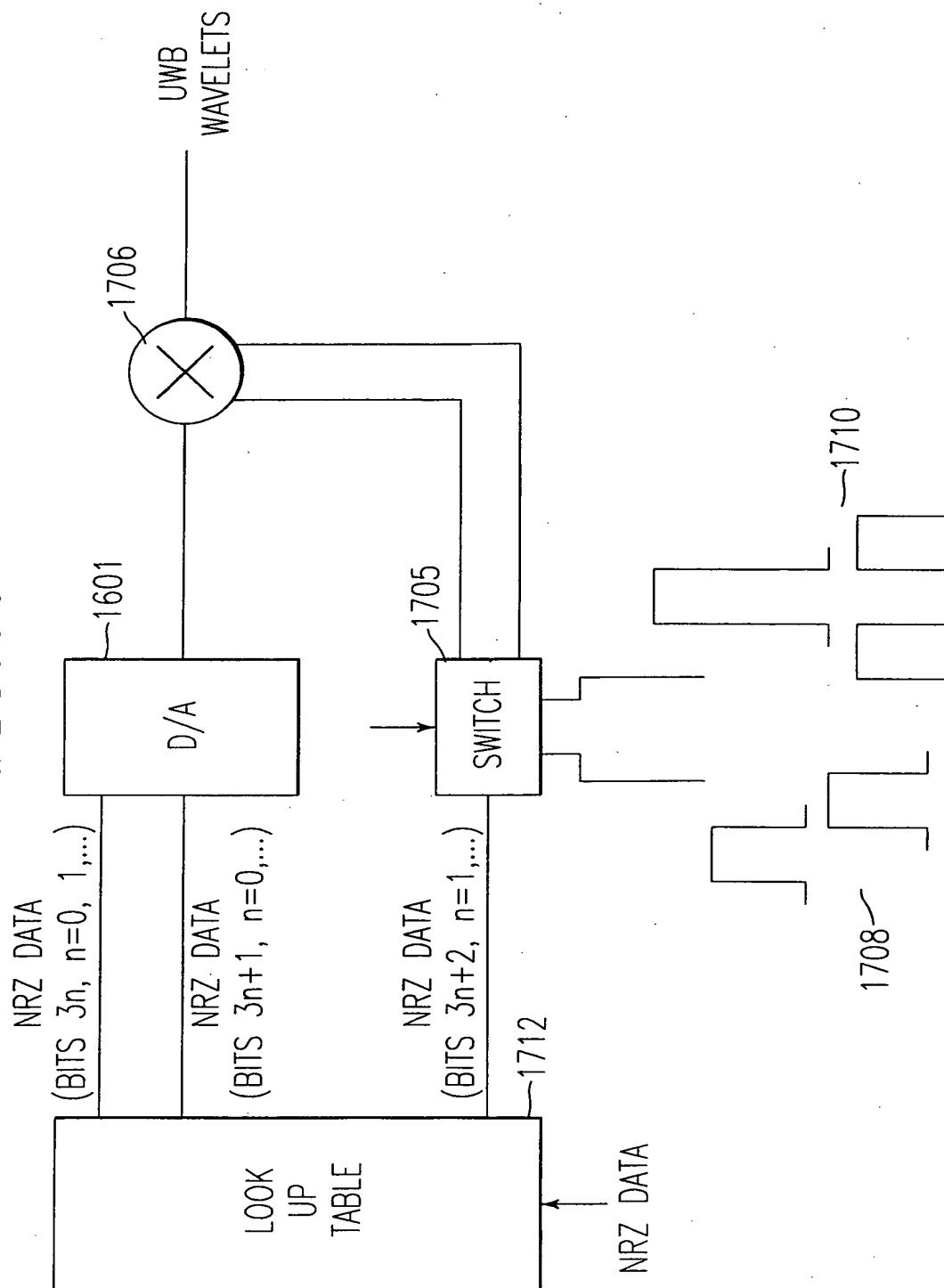




FIG. 19

